REMARKS

Applicants thank Examiner for the indication of allowable subject matter in claims 1, 3, 5-8, 15-17, 20 and 21.

In addition, Applicants have amended claim 2 to correct the reference to the "reset potential." Applicants submit that claim 2 is now also in condition for allowance.

Applicants respectfully request reconsideration of Examiner's rejection of claims 12 – 14, 18, and 19 under 35 U.S.C. §103(a). Examiner has rejected these claims in view of the cited prior art references of *Gowda et al.* (U.S. Patent No. 5,898,168) in view of *Chi et al.* (U.S. Patent No. 5,608,243). Applicants assert, however, that there is no teaching or suggestion to combine the two cited references. In fact, the two references actually teach away from any such combination thereof. *Gowda* teaches to the use of an enhancement mode n-type transistor which is switched on by the application of a positive gate voltage. (see Column 4, lines 66 – 67, and Fig. 5). By applying the positive voltage to the gate over the p-type substrate 56, a channel of electrons is formed between the source and the drain of the transistor and the transistor switches to a conducting state.

On the other hand, *Chi* teaches the use of an enhancement mode p-type transistor which is switched on by the application of a negative gate voltage. (See Column 3, lines 36 – 45). By applying a negative gate voltage to the gate over the n-type well 108, a channel of holes is formed between the source and the drain of the transistor and the transistor switches to a conducting state.

These two references are directed to entirely different transistor types, both of which are

operating in ordinary "enhancement-mode." Accordingly, it impossible to combine the references, as any combination thereof would render the device in an unworkable state. More specifically, the application of a negative gate voltage to operate an enhancement mode p-type transistor device cannot simply be lifted and applied to an n-type enhancement mode device. As there is no teaching or suggestion in either reference to combine, and in fact, such a combination is structurally and electrically unsound, Applicants respectfully request Examiner withdraw his 35 U.S.C. §103 rejection, and place these claims in condition for allowance.

Examiner's remaining references cited but not relied upon, considered either alone or in combination, also fail to teach applicant's currently claimed invention. In light of the foregoing, Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

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